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FACULTY OF ENGINEERING & TECHNOLOGY

BCS-501 Operating System

Lecturer-17

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Memory Management

Basic understanding of Memory Management

MEMORY MANAGEMENT

•To provide a detailed description of various ways of organizing memory hardware

•To discuss various memory-management techniques, including paging and segmentation

•To provide a detailed description of the Intel Pentium, which supports both pure segmentation and segmentation with paging-----

•Program must be brought (from disk) into memory and placed within a process for it to be run

•Main memory and registers are only storage CPU can access directly

•Memory unit only sees a stream of addresses + read requests, or address + data and write requests

•Register access in one CPU clock (or less)

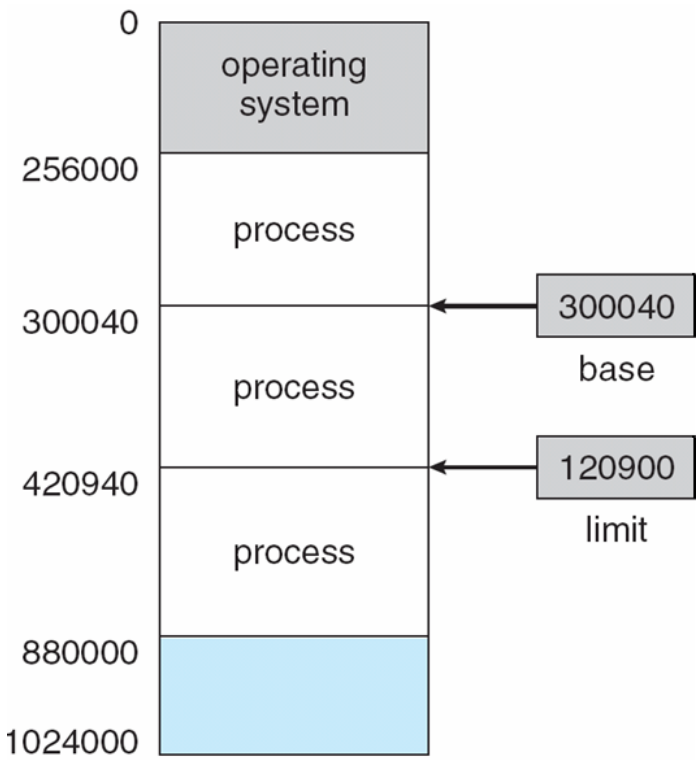
•Main memory can take many cycles, causing a stall

•Cache sits between main memory and CPU registers

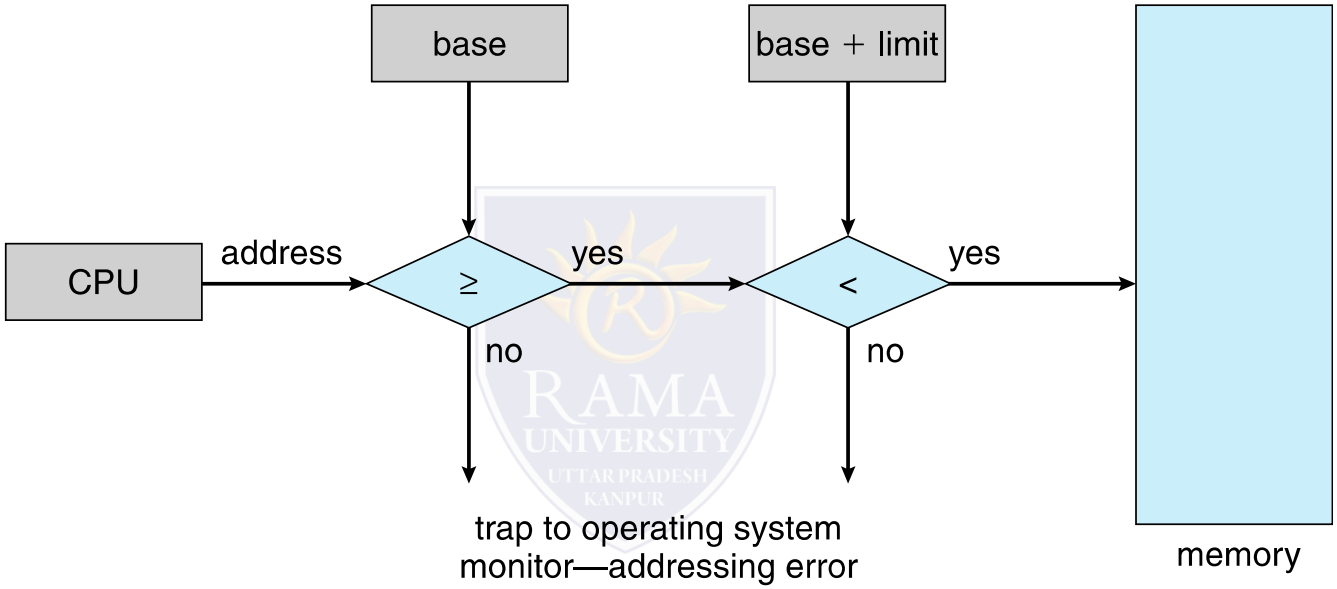
•Protection of memory required to ensure correct operation

Base and Limit Registers

A pair of **base** and **limit registers** define the logical address space
CPU must check every memory access generated in user mode to be sure it is between base and limit for that user



Hardware Address Protection



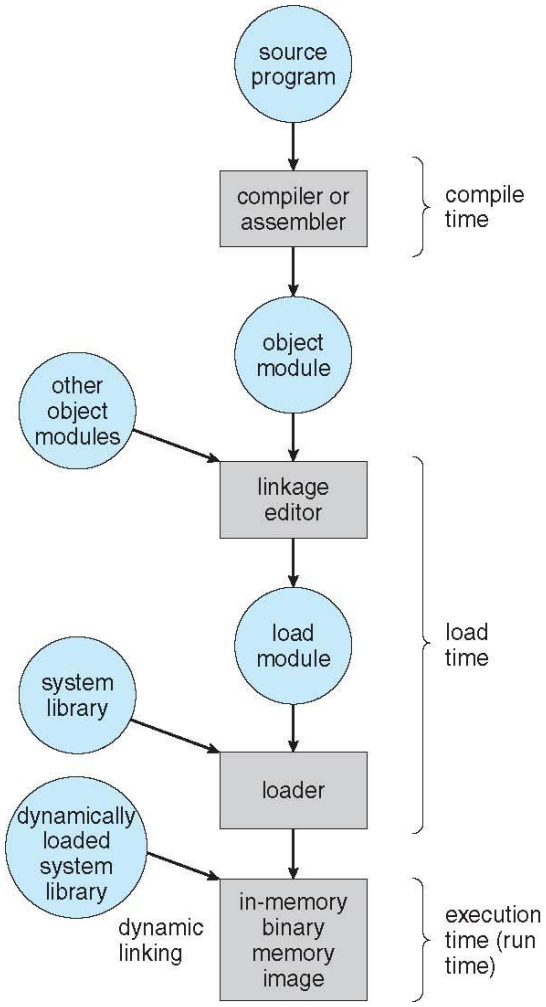
Address Binding

Programs on disk, ready to be brought into memory to execute form an input queue
- Without support, must be loaded into address 0000

Inconvenient to have first user process physical address always at 0000
- How can it not be?

Further, addresses represented in different ways at different stages of a program's life
- Source code addresses usually symbolic
- Compiled code addresses bind to relocatable addresses
  - i.e. "14 bytes from beginning of this module"
- Linker or loader will bind relocatable addresses to absolute addresses
  - i.e. 74014
- Each binding maps one address space to another

Address binding of instructions and data to memory addresses can happen at three different stages
- Compile time: If memory location known a priori, absolute code can be generated; must recompile code if starting location changes
- Load time: Must generate relocatable code if memory location is not known at compile time
- Execution time: Binding delayed until run time if the process can be moved during its execution from one memory segment to another
  - Need hardware support for address maps (e.g., base and limit registers)


source program
compiler or assembler
compile time
object module
other object modules
linkage editor
load module
load time
system library
loader
dynamically loaded system library
dynamic linking
in-memory binary memory image
execution time (run time)

MCQ

CPU fetches the instruction from memory according to the value of:

A. program counter
B. status register
C. instruction register
D. program status word

A memory buffer used to accommodate a speed differential is called

A. stack pointer
B. cache
C. accumulator
D. disk buffer

Which one of the following is the address generated by CPU?

A. physical address
B. absolute address
C. logical address
D. none of the mentioned

Run time mapping from virtual to physical address is done by:
A. memory management unit
B. CPU
C. PCI
D. none of the mentioned

Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called:
A. fragmentation
B. paging
C. mapping
D. none of the mentioned